SSC8151GS6

P-Channel Enhancement Mode MOSFET

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
-50V	±20V	4.5Ω@-10V	-0.13A
		5.8Ω@-5V0	

➢ Description

The SSC8151GS6 is P-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent RDSON with low gate charge. This device is suitable for use in load switch, electronic cigarette and Battery Isolation.

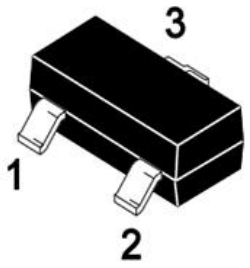
➢ Applications

- Energy Efficient
- Low Threshold Voltage
- High-speed Switching
- DC/DC Converter

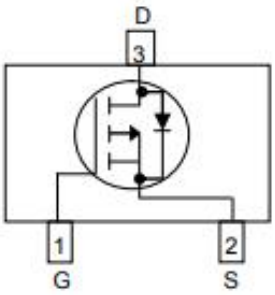
➢ Ordering Information

Device	Package	Shipping
SSC8151GS6	SOT-23	3000/Reel

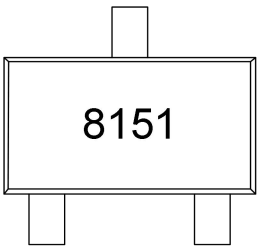
➢ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-50	V
V_{GSS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current [a]	-0.13	A
I_{DM}	Pulsed Drain Current [b]	-0.52	A
P_D	Power Dissipation [c]	225	W
T_J	Operation junction temperature	-55~150	℃
T_{STG}	Storage temperature range	-55~150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	556	℃/W

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

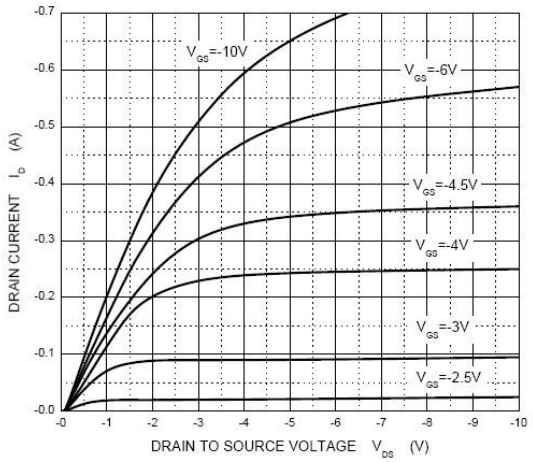
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

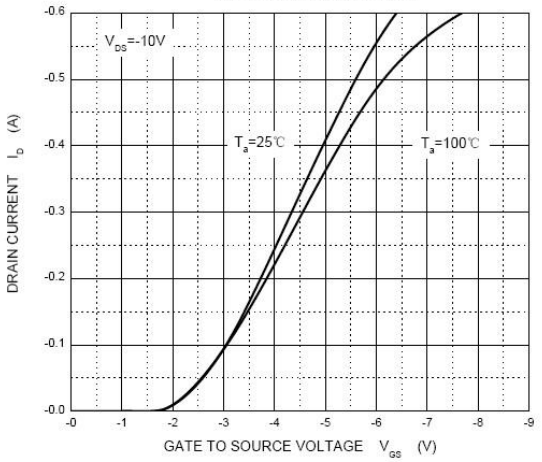
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-50			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-0.9	-1.6	-2.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -0.1A		4.5	8	Ω
		V_{GS} = -5V, I_D = -0.1A		5.8	10	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -25V, V_{GS} = 0V			-0.1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±5	nA
Transconductance	G_{FS}	V_{DS} = -25V, I_D = -0.1A	50			ms
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = -0.13A			-2.2	V
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		30		pF
Output Capacitance	C_{OSS}			10		
Reverse Transfer Capacitance	C_{RSS}			5		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = -15V, I_D = -0.25A, R_L = 50Ω		2.5		ns
Rise Time	T_r			1		
Turn-off Delay Time	$T_{D(OFF)}$			16		
Fall Time	T_f			8		

➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)

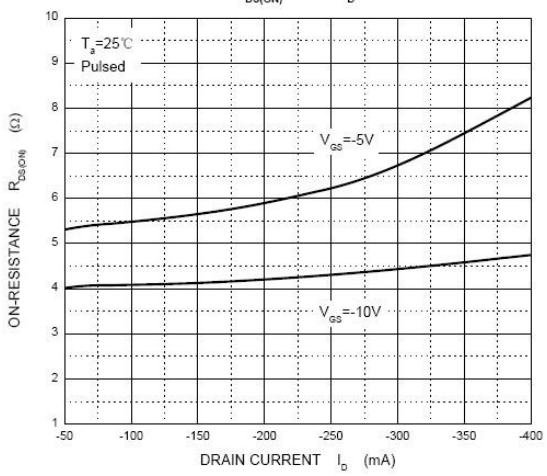
Output Characteristics



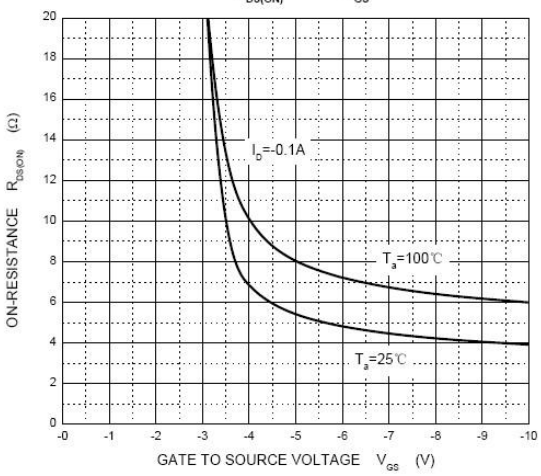
Transfer Characteristics



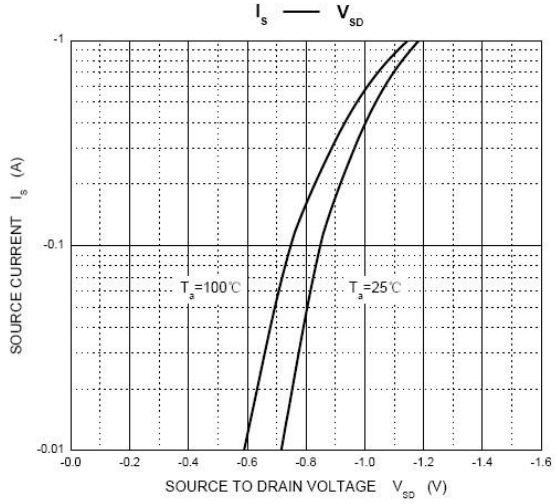
$R_{DS(ON)}$ — I_D



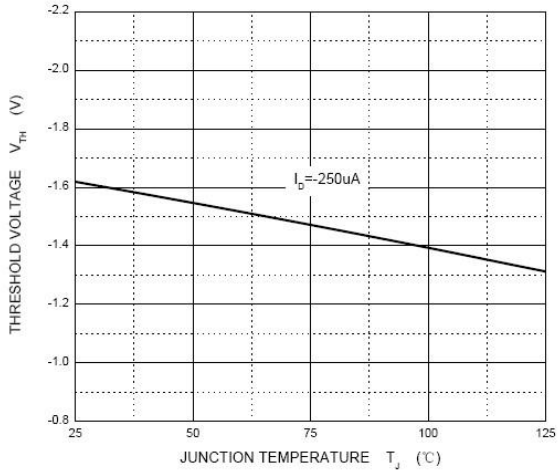
$R_{DS(ON)}$ — V_{GS}



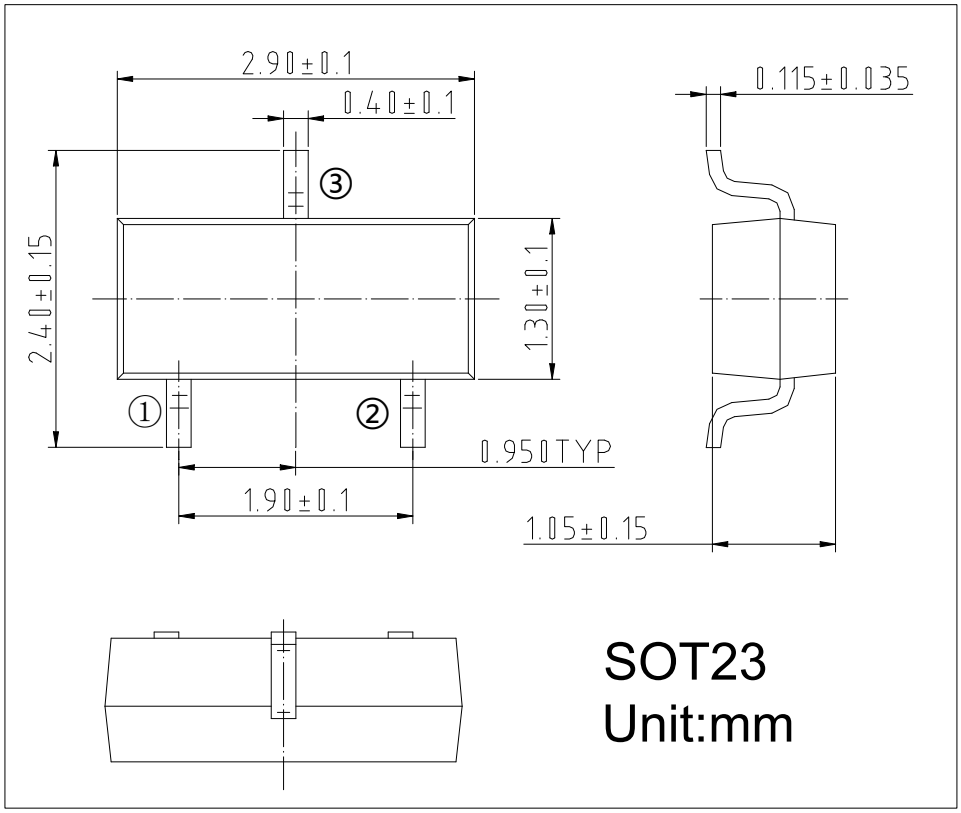
I_S — V_{SD}



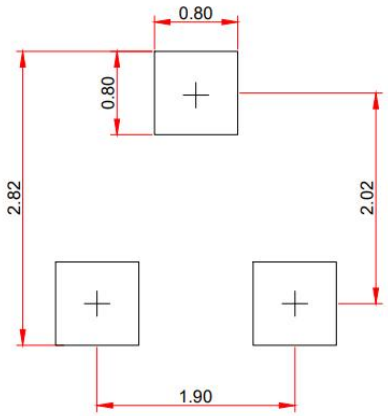
Threshold Voltage



➢ Package Information



Recommended Pad outline (Unit: mm)



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